# A 192×128 Time Correlated SPAD Image Sensor in 40-nm CMOS Technology

# A 192 x 128 Time Correlated SPAD Image Sensor in 40nm CMOS Technology

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***Abstract*—A 192 x 128 pixel single photon avalanche diode (SPAD) time-resolved single photon counting (TCSPC) image sensor is implemented in STMicroelectronics 40nm CMOS technology. The 13 % fill-factor, 18.4 x 9.2 µm pixel contains a 33 ps resolution, 135 ns full-scale, 12-bit time to digital converter (TDC) with 0.9 LSB differential and 5.64 LSB integral nonlinearity (DNL/INL). The sensor achieves a mean 219 ps full-width half maximum (FWHM) impulse response function (IRF) and is operable at up to 18.6 kfps through 64 parallelized serial outputs. Cylindrical microlenses with a concentration factor of 3.25 increase the fill-factor to 42 %. The median dark count rate (DCR) is 25 Hz at 1.5 V excess bias. A digital calibration scheme integrated in a column of the imager allows off-chip digital PVT compensation of every frame on the fly. Fluorescence lifetime imaging microscopy (FLIM) results are presented.**

***Index Terms*— single photon avalanche diode, CMOS image sensor, fluorescence lifetime imaging microscopy. laser ranging.**

## I. Introduction

TCSPC is a photon-efficient, statistical sampling technique whereby photon arrival times are measured relative to a pulsed laser source and are recorded in a histogram over many repeated cycles. Key application areas are in time-of-flight (ToF) range-finding, fluorescence lifetime imaging microscopy, diffuse optical tomography (DOT) and various types of spectroscopy [1]. Conventional instrumentation to implement TCSPC involves photon-counting cards, discrete detectors such as photomultiplier tubes and desktop computers. This bulky and relatively expensive hardware has limited the approach to a few channels, MHz acquisition rates and imaging based on mechanical scanning. More recently CMOS manufacturing has permitted large arrays of SPAD detectors to be manufactured together with timing and signal processing electronics on a single chip.

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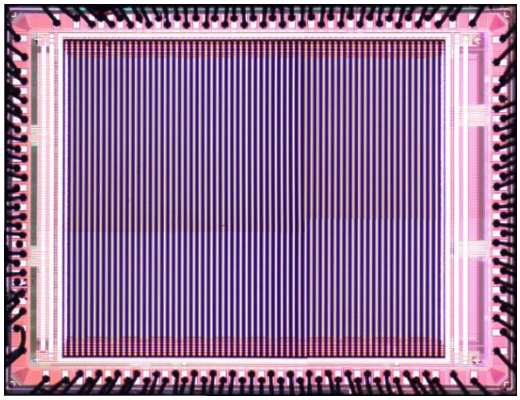


Fig. 1 TCSPC imager micrograph

SPAD arrays together with parallel TCSPC have been the enabling factor in the first high volume quantum photonic consumer applications [2]. Large investment in LIDAR for autonomous vehicles is further propelling CMOS SPAD technology towards advanced nanometre nodes [3] with detector performance approaching that of custom devices.

A number of SPAD image sensors have been proposed permitting TCSPC data to be acquired in parallel from every pixel [4-8]. They provide new capabilities to capture images of light in flight, non-line-of-sight targets, objects through diffuse media, 2-photon FLIM, super-resolved single molecules and time-of-flight depth at various range scales [9-14]. Despite their excellent timing performance, these arrays suffer from low fill-factor (a few percent) or large pixel pitches (40-150 µm) limiting their sensitivity and spatial resolution. A number of recent SPAD image sensors resolve this tradeoff by using event driven dynamic allocation of TDCs either off focal-plane in frontside illumination or vertically stacked [15-16]. The per-SPAD TDC imager architecture is of interest to provide the maximum capacity to convert simultaneous photon arrivals within the same laser cycle such as occur in flash LIDAR on highly reflective targets.

In this paper, we present a SPAD-based TCSPC imager in 40nm CMOS technology with the smallest time to digital converter reported to date (9.2 µm x 9.2 µm) [17]. The 12-bit TDC achieves the finest timing resolution (tuneable from 33 ps to 120 ps) of all reported TCSPC pixels at an energy efficiency figure of merit (FoM) of 34 fJ/conv and <1LSB DNL and <6LSB INL. The photon detection efficiency (PDE) of the array has been enhanced with cylindrical microlenses to

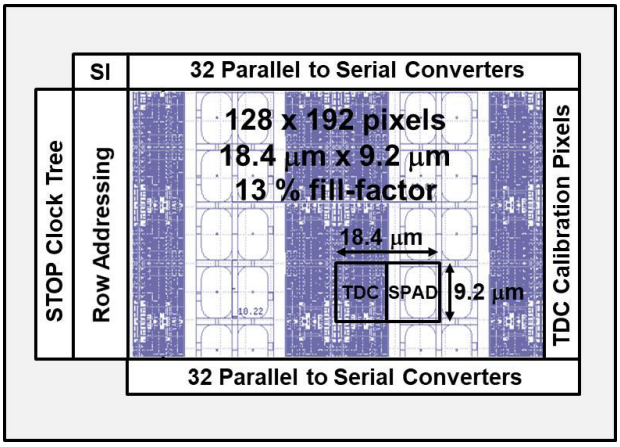
provide a mean concentration factor of 3.25 and a 42% effective fill-factor. The sensor also has a very low median DCR of 25 Hz obtained at 1.5 V excess bias and at room temperature conditions. SPADs have a peak PDP of 34% at 560 nm for 1 V excess bias at room temperature [3] and a quench time of 5 ns.

This combination of high sensitivity, low noise and precise timing resolution offers a transformative capability to low-light time-resolved wide-field microscopy where sensitivity is paramount to image very dim samples and the contrast of lifetime is the key requirement to answer many biological questions. The sensor improves on the architecture proposed in [4] by trading off lower frame rate and jitter for a higher pixel sensitivity and resolution. Indeed, many practical applications of FLIM demand video frame rate and few 100ps contrast between multiplexed fluorophores with lifetimes in the 2-10ns range. In addition, the 18kfps of timestamped pixel corresponds to the typical photon arrival rates typical of dim microscopic scenarios thus minimizing pile-up loss.

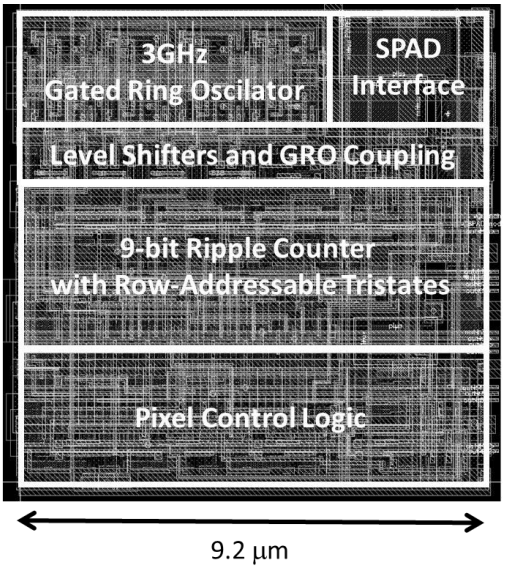
The maximal TDC full-scale range of 490 ns also enables ToF laser ranging applications up to 73.5m distance. The imager integrates an on-chip calibration scheme using a column of the imager which continuously measures full-periods of a clock to allow off-chip digital PVT compensation of every TCSPC frame on the fly. Full characterisation results of the sensor are presented as well as FLIM images.

## II. Sensor Design

A micrograph of the sensor is shown in Fig. 1. The 3.15 mm x 2.37 mm chip is integrated in STMicroelectronics 40 nm CMOS technology offering industrialized SPADs [3]. The sensor block diagram in Fig. 2a consists of addressing circuitry, 64 parallel to serial converters and a 192 x 128, 18.4 µm x 9.2 µm pixel array. Each pixel comprises a TDC coupled to a SPAD. The last column of the pixel array implements a calibration scheme to allow off-chip digital PVT compensation of every frame on the fly. A serial interface (SI) allows configuration of the sensor in multiple modes such as TCSPC and photon counting as well as optional enabling and disabling of selectable pixel rows and columns. A column pair wise SPAD well sharing layout strategy (Fig. 2a inset) is adopted to optimize fill-factor and allow future 3D stacking at a regular 9.2 µm pitch [18]. The sensor operates with greatest photon efficiency at a maximum frame rate of 18.6 kfps with laser repetition rates of around 2 MHz (assuming the conventional 1% pile-up limit).




(a)




(b)

Fig. 2 (a) Sensor block diagram. (b) Pixel layout.

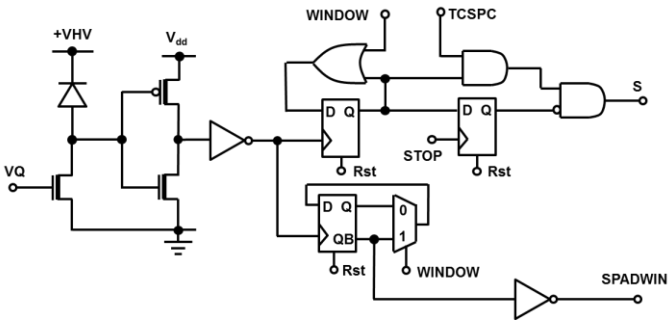



Fig. 3 SPAD interface, gating and TDC control circuitry

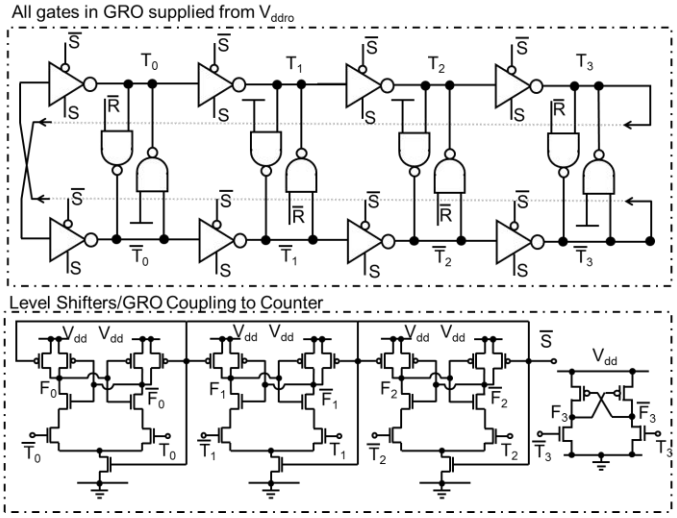



Fig. 4 TDC core circuit

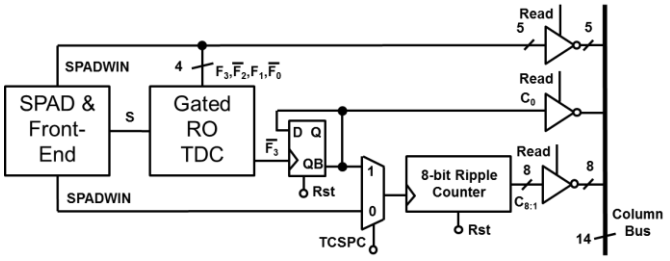



Fig. 5 Pixel circuit and readout

### A. *Circuit Architecture.*

A highly optimized version of the pixel architecture originally proposed in [4] has been implemented in order to attain a pitch compatible with scientific imaging or ToF applications and scalable to megapixel resolutions. This involves dispensing with any functions that are not necessary in the pixel and re-using hardware resources wherever possible. In particular, the d-type flip-flop found in the digital cell library has been optimized to remove redundant re-buffering of clock signals and outputs. This saves over 30% of the dominant area contributor to the pixel.

The circuits interfacing the SPAD to the TDC and photon counting functions are shown in Fig. 3. The layout of the pixel overlaid to show the different blocks is shown in Fig 2b. A single thick oxide 3.3 V NMOS biased with a global gate voltage *VQ* passively quenches the SPAD. SPAD pulses are level shifted to the 1.1V digital $V_{dd}$ by a thick oxide inverter. All other circuits exploit the digital 40 nm transistors.

In TCSPC mode (*TCSPC*=1), a compact edge-sensitive trigger circuit generates an enable signal S for the TDC by means of a pair of d-type flip-flops. The first flip-flop will latch a 1 on the rising edge of the first SPAD pulse falling within the exposure period and coincident with a high state of *WINDOW* signal (time between *Rst* pulses) starting the TDC. The second flip-flop resets *S* to 0 on the next rising edge of the *STOP* waveform provided that the TDC has been started. In this way, the *WINDOW* signal achieves global electrical masking of photons events allowing suppression of ambient background in LIDAR applications or dark count events in FLIM. In particular, this reduces the likelihood that precious TDC resources are expended on photons likely to be uncorrelated with the laser excitation.

In photon counting mode (*TCSPC*=0), another d-type flip-flop toggles on the rising edge of the SPAD pulse only if *WINDOW* is high generating the *SPADWIN* signal. This signal also acts as the least significant bit of the photon count. In this mode, the *WINDOW* signal provides a global electrical masking on light intensity. This allows either global shutter imaging with zero parasitic light sensitivity or single photon synchronous detection (SPSD) operation [19] when operated over a number of frames and quadrature *WINDOW* gates.

Fig. 4 shows the TDC circuit which consists of a 4-stage pseudo-differential gated ring oscillator (GRO), level shifting and coupling stages [4]. The ring oscillator core is supplied from a separate power rail $V_{ddro}$ to allow global external tuning of the TDC resolution. The separate $V_{ddro}$ power rail also minimizes coupling of this critical high frequency timing reference to unrelated activity of other digital functions on the chip such as row addressing and readout. Both $V_{ddro}$ and $V_{dd}$ are gridded up to the thick low-resistive top metal layers (metal 6 and 7) at maximum width and smallest spacing permitted by the design rules and fill-factor requirements.

Setting signal *R* high resets the TDC to an initial condition. The rising edge of signal *S* starts the ring oscillator that operates over a range 2-4 GHz depending on the $V_{ddro}$ setting. At the instant the signal *S* falls the nodes $T_{3:0}$ and $\overline{T}_{3:0}$ regenerate to memorize the internal state of the oscillator. The state of these internal nodes is used to provide the three least significant bits (LSBs) of the TDC by a decoding operation performed in software. Three balanced dynamic comparators act to level shift the states of $T_{3:0}$ from $V_{ddro}$ to $V_{dd}$ whilst reducing the loading on the loop to only two floating NMOS transistors. A cross-coupled level shifter couples $T_3$ and $\overline{T}_3$ to the first stage of a ripple counter and resolves potential metastability issues when *S* falls at the same instant as a positive transition on $T_3$.

The main pixel schematic integrated in a 9.2 µm x 9.2 µm area is shown in Fig. 5. An 8-bit ripple counter is multiplexed either to act as a photon counter or to count oscillator periods to extend the dynamic range of the TDC. In TCSPC mode, a dedicated high-speed toggle flip-flop immediately divides the ring oscillator frequency to allow this high-speed signal to pass the multiplexer. Thus, the coarse LSB in TCSPC mode ($C_0$) and the LSB in photon counting mode (*SPADWIN*) are derived from two different flip-flops. Tri-state inverters controlled by a row read signal drive the 14-bit state of the pixel onto a column output bus under control of the row addressing circuit.

### B. *TDC Calibration*

It is well known that gated ring-oscillator TDC resolution is strongly influenced by power supply voltage and temperature [20-21]. Fig. 11 shows that variation of the $V_{ddro}$ power supply from 0.7 V to 1.2 V changes the TDC resolution from 112 ps to 33 ps. In addition, a standard deviation of around 1% in the LSB has been determined across a single column. The wide TDC resolution tuning range is a useful feature to extend the dynamic range of the sensor for different fluorescence lifetimes or ToF distances. However, it also represents an uncertainty of the achieved time resolution in the case of

unknown process, voltage and temperature variations affecting the ring oscillator. A column of pixels on the right side of the imager continuously measures full-periods of the *STOP* clock to allow off-chip digital PVT compensation of every frame on the fly.

These particular pixels, henceforth known as calibration pixels, occupy alternating rows of the right-most column of the pixel array, for 96 calibration pixels. When enabled, the TDC data from the calibration column is read-out of the chip in place of the last four right-most ordinary pixel columns. The TDC in the test pixels differs from the imaging pixels by having the STOP clock connected in place of the SPAD anode in the imaging pixels. The TDC is started by the rising edge of the STOP clock and stopped by the rising edge of the subsequent STOP cycle, thus timing the period of the STOP clock.

The 64 parallel input to serial output (PISO) converters read out the data from each of the pixels in a rolling row readout scheme. 32 top and bottom PISOs read out respective half columns of the array. Each PISO reads out 4 pixel columns from each row as shown in Fig. 6.

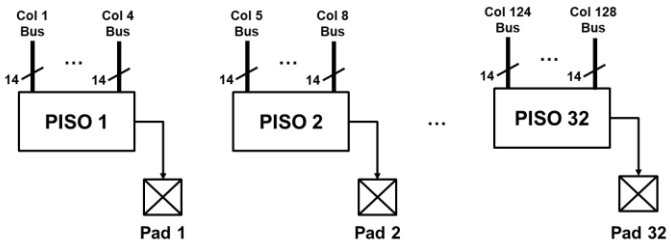



Fig. 6 PISO readout diagram.

### C. Sensor Operation

Two exposure modalities are possible; high temporal aperture ratio (TAR) [22] rolling or parasitic light insensitive global shutter. In the former, pixels are read and reset using a rolling shutter scheme with minimal motion artefacts due the high frame rates. A token-passing row shift register reads pairs of rows of the pixel array from the central rows outwards in a rolling cycle and operates continuously at up to 18.6 kfps. An arbitrary pattern of rows can be read-out at a faster frame rate upon identification of regions of interest. At any time only the currently two addressed rows of the pixel array are not in integration achieving a TAR of 99% that is essential for low light imaging applications.

Upon triggering and timing a single photon, each TDC is dead and unavailable to detect subsequent photons within the same exposure before readout. High illumination conditions and long exposures could decrease the effective TAR due to pixels firing at the start of the exposure and being inactive for the remaining temporal aperture. This effect is negligible due to the low light operating conditions of FLIM. On the other hand, longer exposures increase the probability of triggering more TDCs to avoid reading out empty frames. Adjusting the readout frequency and thus the exposure period in response to the illumination conditions can be used to optimise the TAR while maximising the probability of reading out triggered pixels from each frame.

In global shutter mode, the *WINDOW* signal is used to enable TCSPC or photon counting within arbitrary frame durations. In TCSPC mode (Fig. 7) a laser is pulsed in synchrony with the *STOP* pulse distributed to the whole array via a clock tree. The TDC will only start up if the rising edge of the SPAD pulse is contained in the *WINDOW* high period. Only the first such photon will be captured within an exposure period. In photon-counting mode, photons will be integrated precisely within the *WINDOW* high period which allows exposure times to be set from nanoseconds to seconds time scales.

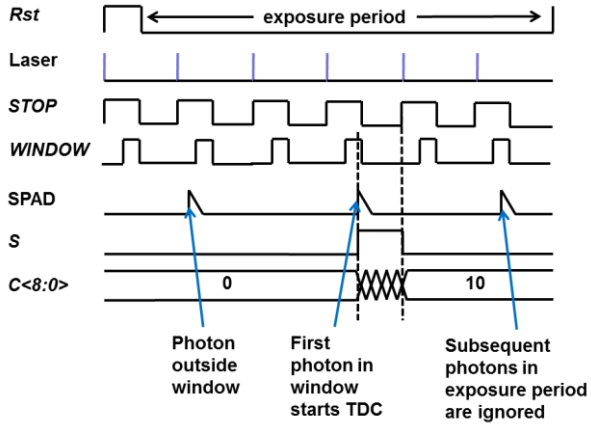



Fig. 7 Sensor operation in TCSPC mode

Banks of 32 parallel to serial converters at the top and bottom of the array each convert 4 columns of 14-bit data into a 56 bit serial sequence to 64 I/O pads at a maximum rate of 100 MHz. The readout time of an entire frame is therefore 54.76 µs.

## III. Sensor Characterization

The TDC INL and DNL are measured using a code density test with ambient light providing a random input to populate a histogram with over 300 k photon time stamps. The DNL/INL plot of a typical pixel is shown in Fig. 8 with the TDC operating at nominal $V_{ddro}$=1.1 V over 140 ns (92.5% of full-scale at this voltage).

The IRF of a typical pixel is measured using a Hamamatsu PLP-10 685 nm laser diode in Fig. 9. The SPAD is biased at 1.5 V excess bias and a typical jitter characteristic with a diffusion tail [3] and FWHM/100 of around 1 ns is observed.

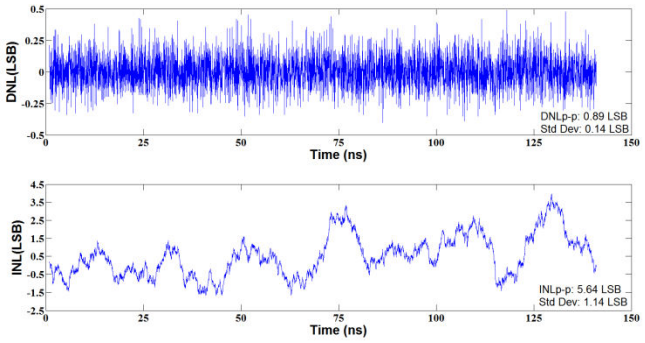



Fig. 8 Typical TDC INL and DNL plots over 140 ns

A map of IRFs of the full-pixel array is shown in Fig. 10 with IRF of hot pixels set to 0 (highlighted in blue) and removed from calculations. The mean pixel FWHM jitter is 219 ps with a variance of 26.7 ps. This is close to the native jitter of the SPAD of 170 ps [3] suggesting around 138 ps is due to the laser (FWHM = 70-100 ps) and the TDC. The deviation on the TDC LSB at full TDC range is 45 ps for nominal TDC operating conditions. The SPAD median DCR is measured to be 25 Hz at a 1.5 V excess bias and at room temperature conditions. Each SPAD has a 22 $\mu m^2$ active area implying a 1.14 $Hz/\mu m^2$ median DCR.

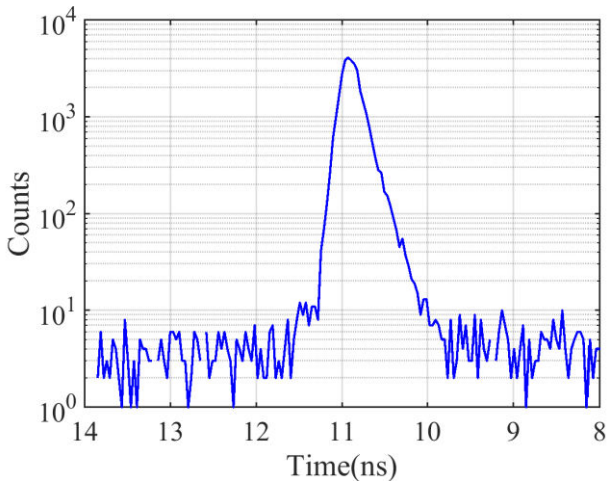



Fig. 9 Typical IRF of a single pixel

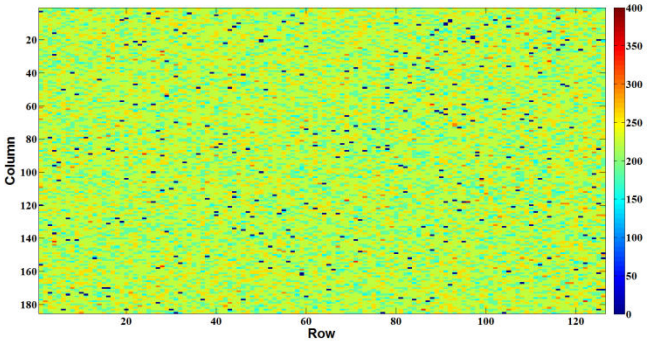



Fig. 10 IRF FWHM map of entire array. IRF of hot pixels set to 0 and highlighted in blue.

The TDC resolution as a function of ring oscillator supply voltage $V_{ddro}$ is measured using the calibration column. The results reported in the graph in Fig. 11 show a TDC resolution varying from 33 ps to 112 ps when varying $V_{ddro}$ from 1.2 V to 0.7 V.

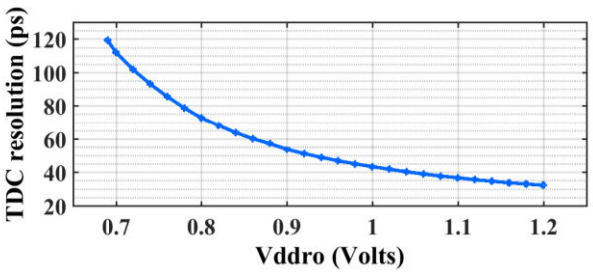



Fig. 11 TDC resolution vs power supply voltage

The TDC data reported by the calibration column is used to calibrate off-chip the TDCs of the imaging pixels. To test the TDC calibration of the pixels in response to ring oscillator supply voltage variation, the IRF of a Hamamatsu PLP-10 654 nm laser diode is measured at different $V_{ddro}$ values from 1.2 V to 0.75 V in steps of 100 mV. The uncalibrated TDC data shows a shift in the IRF across the histogram bins in Fig. 12 consistent with the varying TDC resolution across the voltage values. Increasing $V_{ddro}$ results in a narrower bin size, thus the same laser pulse is shifted to a higher bin position in the histogram. The width of the histogram IRF also increases with increasing $V_{ddro}$ in line with a narrower bin width. A Hamamatsu C10196 Picosecond Light Pulser is used to drive the laser and provide a 10 MHz STOP clock to the sensor. The calibration pixels output the TDC data corresponding to the measurement of the STOP clock period. This is used together with knowledge of the STOP clock frequency to calculate the TDC LSB resolution. The TDC resolution computed by the calibration columns for each voltage step allows correcting for the voltage-dependent time shift in the IRF and distortions in the histogram. By multiplying the imaging pixel TDC data by the reported resolution of the calibration pixels the IRF are shown to align in Fig. 13. Fig. 14 shows the centroid of the pixel IRF before and after applying the TDC calibration to the collected TCSPC data. The calibrated IRF centroid undergoes a deviation of 75 ps across the $V_{ddro}$ range (blue trace in Fig. 14), a factor of 100 improvement on the maximum voltage-induced IRF centroid variation in the non-calibrated histogram (red trace in Fig. 14). Though not demonstrated here, the same calibration can be extended to correct for process and temperature-dependent variations in the TDC resolution.

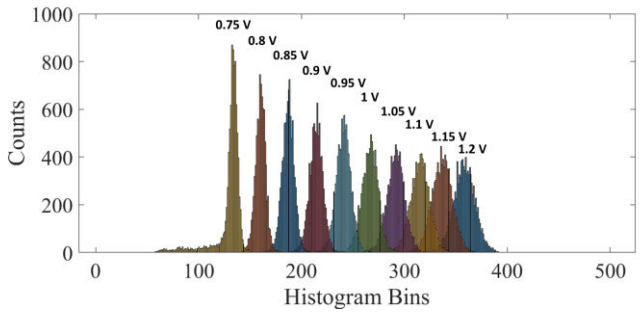



Fig. 12 IRFs of a single pixel for different $V_{ddro}$ values from 0.75 V to 1.2 V showing shift due to varying TDC resolution.

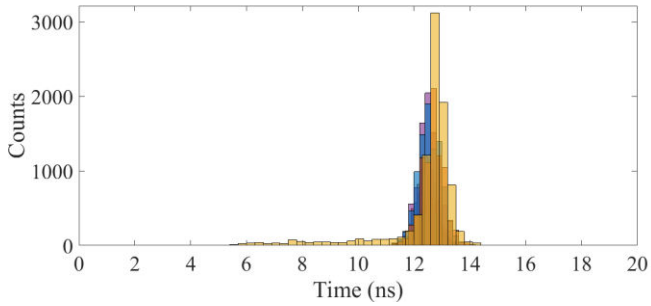



Fig. 13 IRFs of a single pixel for different $V_{ddro}$ values from 0.75 V to 1.2 V after applying TDC calibration correction to account for changing TDC resolution. IRFs now overlap.

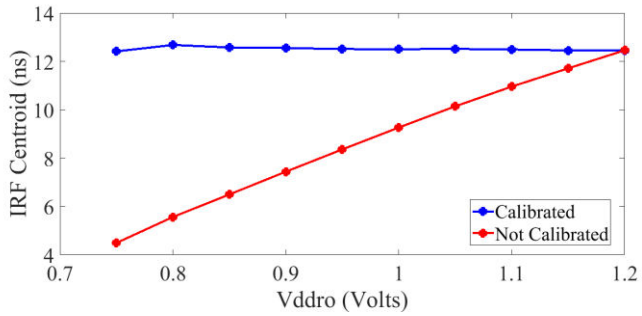



Fig. 14 IRF centroid of a single pixel for different $V_{ddro}$ values from 0.75 V to 1.2 V before and after applying TDC calibration.

A single calibration pixel is sampled for 10000 cycles with $V_{ddro}$ set to 1.1 V to determine the deviation of the measured TDC LSB over multiple calibration cycles. The TDC LSB distribution of a single calibration pixel has a standard deviation 0.087 ps as shown by Fig. 15. Fig. 16 shows the distribution of the TDC LSB sampling the whole calibration column, comprising 96 pixels, over 10000 calibration cycles. The standard deviation in the TDC LSB when sampling the entire calibration column increases to 0.401 ps, 1% of the TDC LSB. A low deviation in the calibration column TDC LSB means that samples from all calibration pixels can be combined to obtain a single calibration factor to correct for PVT-induced histogram distortions in the imaging pixel data as shown in Fig. 12 and 13. Combining the calibration data from all pixels in the calibration column reduces the time required to collect enough samples to calculate the reference TDC LSB resolution for the TCSPC histogram data, thus being able to perform calibration on-the-fly with a maximum of 96 calibration samples per frame. The number of samples required for effective calibration depends on the sensor application and the expected variations. As calibration TDCs are also affected by ring oscillator accumulated jitter, a higher number of samples might be required when using a low frequency STOP clock for calibration. Temperature variations from on-chip power consumption, in turn determined by the illumination intensity, might also require more frequent calibration cycles to monitor temperature-related TDC LSB variations.

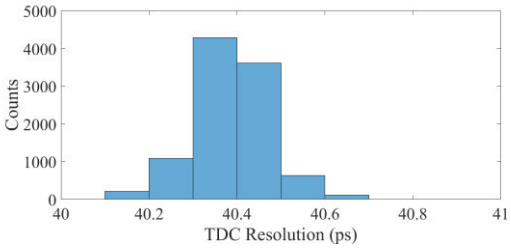



Fig. 15 TDC LSB distribution of a single calibration pixel for $V_{ddro}$ = 1.1 V.

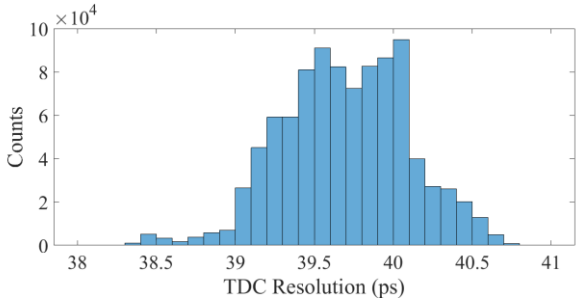
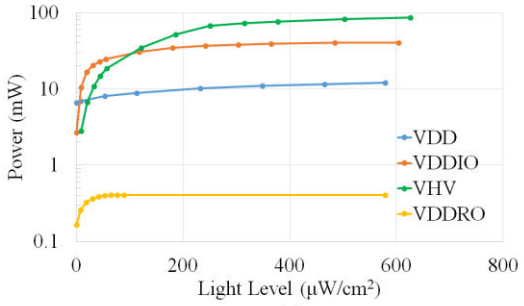
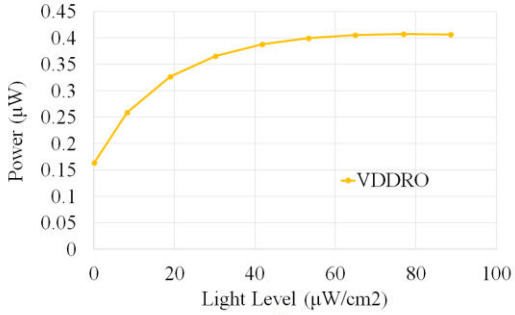



Fig. 16 TDC LSB distribution of 96 calibration pixels for $V_{ddro}$ = 1.1 V.

Measurement of the power consumption of the sensor on each of the chip supplies as a function of the incident illumination is shown in Fig. 17a. As expected the power consumption of such an array is proportional to light level. The low duty cycle operation of the TDCs shows a negligible power consumption of the ring oscillators saturating at 0.41 mW with a power consumption per TDC of 16.5 nW on $V_{ddro}$. The dominant contributors being 90mW for the SPADs, 10mW of the core electronics supply and 3mW I/O power for a maximum total sensor power consumption of 140 mW under high illumination. The power consumption on the ring oscillator supply shown in Fig. 17b shows the power increasing with light level due to an increasing number of TDCs triggered per frame. $V_{ddro}$ saturates at the level corresponding to all pixel TDCs triggered within a 10 MHz STOP clock period. Power consumption measurements are presented for a light intensity sweep reaching an illumination level orders of magnitude higher than would be expected in FLIM applications. The sensor power consumption for all supplies would be expected to lie in the linear regions of the curves in Fig. 17 rather than at peak power saturation, expecting a total sensor power consumption less than 10 mW for count rates below the sensor pile-up limit.




(a)




(b)

Fig. 17 (a) Power consumption on the core supply $V_{dd}$, I/O supply $V_{ddio}$, SPAD cathode supply $V_{HV}$ and ring oscillator supply $V_{ddro}$. (b) Power consumption on the ring oscillator supply $V_{ddro}$.

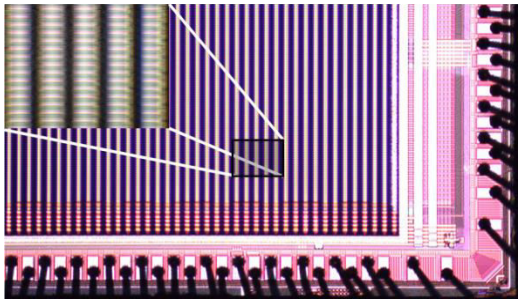


Fig. 18 Photomicrograph of the microlensed sensor

Cylindrical microlenses have been implemented on a per-die basis [23] achieving a mean concentration factor of 3.25 (Fig. 18) and increasing the effective SPAD fill factor from 13% to 42%. These microlenses focus light onto a pair of SPADs between a column of two TDCs as shown in Fig. 19. Some light is lost in the n-well isolation region between the two shared-well SPAD rows.

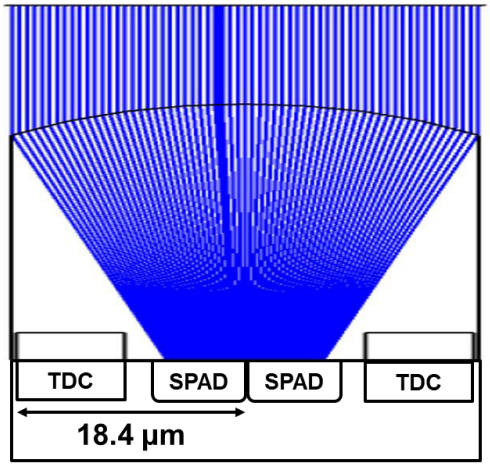



Fig. 19 Microlens ray tracing design with layout of SPAD and TDC.

## IV. Fluorescence Lifetime Imaging

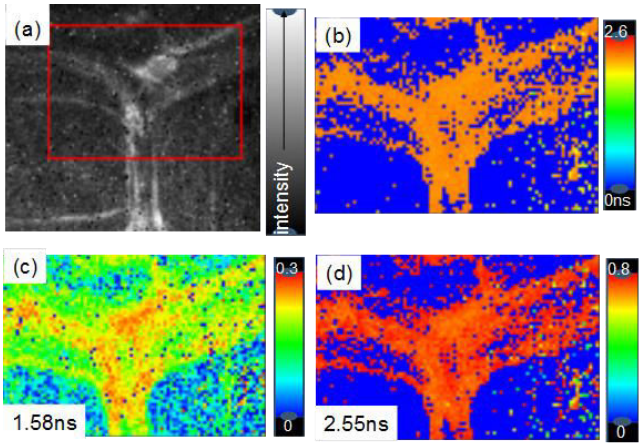



Fig. 20(a) Photon counting fluorescence image of DASPMI stained onion cells, (b) average lifetime, (c) and (d) normalized pre-exponential components. The data was obtained in ~2s.

In order to demonstrate wide field FLIM, onion cells stained with the dye DASPMI [24] were studied on a microscope set up using a HORIBA Scientific DeltaDiode DD-485L laser as the excitation source. The SPAD array was packaged into a camera module referred to as QuantiCam and integrated into commercial FLIM software and mounted on a simple microscope demonstration system. The HORIBA Scientific EzTime Image software enables a "region of interest" to be selected in the photon counting intensity image (see Fig. 20a, where the red box indicates the region selected). TCSPC data were just collected from pixels in the region of interest. This showed an area including the cell walls. The lifetime data were analyzed globally using the EzTime software as the sum of two exponentials and lifetimes of 1.58 ns and 2.55 ns were obtained. Maps showing the average lifetime (Fig. 20b) and the normalized pre-exponential components for each of the lifetimes are given in Fig 20c,d. This shows that the longer-lived decay component is predominately associated with the cell wall and provides a contrast to the cell interior.

Widefield FLIM acquisition with the Quanticam is compared to scanning FLIM using a modified HORIBA Scientific DynaMyc (including FiPho timing electronics, DeltaDiode laser excitation and HPPD-720 detection). In both cases data were collected and analyzed using EzTime Image software. Although, theoretically the Quanticam's parallel data acquisition can collect images 24,576 times faster, a "real world" measurement on a sample to the same precision (225 million photon events and a similar peak histogram count) was made using a Convallaria root sample.

The outcome of these measurements is shown in Fig 21. The time to collect the data with the scanning system was ~ 16 minutes, while the equivalent measurement using the QuantiCam on a simple microscope demonstrator took 15 seconds. Thus even on a very simple set up the QuantiCam can collect data orders of magnitude faster than a conventional scanning system.

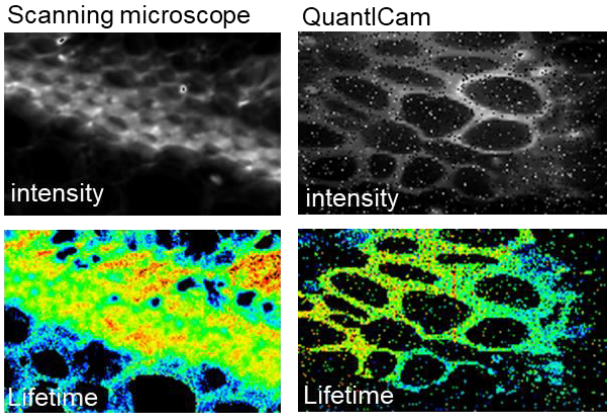



Fig. 21. Comparison of both intensity and average fluorescence lifetime data taken with a scanning microscope and the QuantiCam. The precision was ~225M photon events and the scan required 16m to acquire compared to 15s for the QuantiCam.

To further investigate the potential for fast-FLIM acquisition a test was performed taking into account the report that >185 photon events are required for a basic analysis of TCSPC data [25]. Measurements with different data acquisition times were taken on the Convallaria sample and the images accessed to check that sufficient pixels contained over 200 photon events in order to facilitate data analysis. Fig 22 shows the image quality obtained with a data acquisition time of 100 ms. It should be noted that both permanently on or dead pixels can be masked or removed from the image using the acquisition software (EzTime Image) and thus not contribute to the fitting of the lifetime data. However, this can give rise to the speckle effect seen in some of the FLIM data and at this point no attempt has been made to disguise this by interpolation of the data from surrounding pixels. Also, no correction has been made for the fact that the pixel size is not the same in both x and y directions. This can simply be corrected by adjustment of the resultant image aspect ratio. For the purposes of this work we show the "raw" images produced by the device to illustrate its potential.

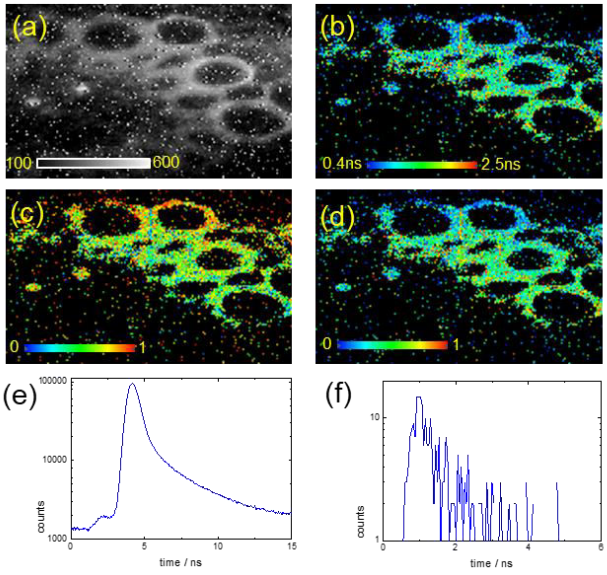



Fig. 22 (a) TCSPC intensity image acquired in 100 ms, (b) average lifetime just calculated in pixels with >200 photon events, (c) and (d) normalized pre-exponential images for the lifetime components (0.39ns and 2.52ns) obtained from a 2 exponential global analysis of the image. (e) histogram of the sum of all the selected pixels and (f) histogram from a single pixel located at the cell wall.

Table I shows a comparison of QuantiCam with other SPAD imagers with per-pixel TDC. Our device is integrated in the most advanced CMOS technology node resulting in the smallest TDC and pixel pitch while at the same time providing the highest fill-factor after microlensing. The technology node also makes it possible to achieve a finer time resolution at a comparable energy efficiency figure of merit to other sensors. The 12-bit dynamic range has been chosen to allow the TDC to cover practical time ranges for common organic fluorescent dyes as well as outdoor time of flight ranges. The low dark count rate of 25 Hz at 1.5 V excess bias is at a practical level for microscopy and could readily be improved by cooling. Time gating the TDC in a range of interest where the signal is located can further reduce the impact of DCR on the signal to noise ratio. The percentage of hot pixels is considerably higher than other solid-state low light imaging technologies for microscopy and still represents an impediment to the use of SPAD imagers in these applications. Average power consumption of the sensor is extremely low as the TDCs are only active at a low duty cycle (typically <0.1%). On the other hand, the peak power consumption of such a GRO based architecture is potentially very high (Watts) in the case that all the TDCs become active in the same instant. Such a scenario which occurs if the laser is directly incident on the sensor is however not a relevant microscopy use-case.

* FoM= peak power x precision **Estimated based on total core power

Table 1. Comparison of SPAD imagers with per-pixel TDC

| Parameter | This Work | [7] | [6] | [4] | [5] |
|---|---|---|---|---|---|
| Process | 40 nm | 150 nm | 350 nm | 130 nm | 180 nm |
| Pixel | | | | | |
| Pixel pitch (µm) | 18.4 (x) 9.2 (y) | 44.64 | 150 | 50 | 64 |
| SPAD dia. (µm) | 5.4 | 19.8 | 30 | 6 | 12 |
| SPAD shape | Square, rounded corners | Square | Circular | Circular | Circular |
| Fill factor (%) | 13 (42) | 19.48 | 3.14 | 1.2 | 2.7 |
| Median DCR (Hz)/Veb (V) | 25/1.5 | 600/3 | 120/6 | 50/0.73 | 42000/1 |
| TDC | | | | | |
| Area ($\mu m^2$) | 84.6 | 402.7 | 21793 | 2244 | 812 |
| Range (ns) | 135–491 | 53 | 360 | 55 | 297 |
| Resolution (ps) | 33-120 | 204.5 | 350 | 55 | 145 |
| Depth (bit) | 12 | 8 | 10 | 10 | 11 |
| $DNL_{p-p}$ (LSB) | 0.9 | 1.5 | 0.04 | 0.6 | 0.55 |
| $INL_{p-p}$ (LSB) | 5.64 | 2.17 | 0.20 | 4 | 3 |
| Precision (ps) | 208 | 205 | 254 | 170 | 435 |
| FoM* (pJ/conv) | 0.034 | 0.12** | 0.088** | 0.034 | 0.67 |
| Chip | | | | | |
| Array size | 192x128 | 32x32 | 32x32 | 160x128 | 64x64 |
| Chip size (mm) | 3.2x2.4 | 1.7x1.9 | 9x9 | 11x12.3 | 5x5 |
| Frame rate (fps) | 18.6k | 80k | 100k | 50k | 5k |
| Power (mW) Core / IO | 1 / 30 | 11.1 | 400 / 25 | 500 | 2.7 |

## V. Conclusion

Advanced nanometer CMOS nodes provide TDC pixels with practical pitch and fill-factor for high-resolution imaging. The sensor enables parallel TCSPC and multi-exponential FLIM at two orders of magnitude faster acquisition rates than scanning systems. Enhanced PDE and low DCR offer competitive

imaging performance with widefield microscopy cameras at far superior time resolution.

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